

REMARKS

An obvious minor error in the specification has been corrected. This application contains claims 1 -20.

Claims 1-20 were rejected under 35 U.S.C. 101. Claims 1 and 11 have been amended herein to be directed to the execution of a computer program. After examining the tag associated with a given instruction, and if such associated tag has been set, branching to the translated version of the given instruction, for further execution of the program occurs. The execution of a computer program is exactly the type of "useful, concrete and tangible result" contemplated by the United States Court of Appeals for the Federal Circuit in State Street Bank & Trust C. v. Signature Financial Group, Inc., 47 U.S.P.Q.2d 1596. It is thus submitted that claims 1-20 are directed to patentable subject matter, under 35 U.S.C. 101.

Claims 1-20 were rejected under 35 U.S.C. 102(e) as being anticipated by Bala. In view of the amendments made herein, and the remarks below, these rejections are respectfully traversed.

Applicants' invention, as set forth in claim 1, as amended herein, is directed to in a computing system that includes dynamic compilation capability, a method for controlling the execution of an instruction of a computer program. The method comprises the steps of translating an instruction from a first representation to a translated representation, and setting a tag associated with the

instruction in the first representation; and prior to execution of a given instruction in the first representation, examining the tag associated with the given instruction, and if such associated tag has been set, branching to the translated version of the given instruction, for further execution of the program. Significantly, the examining of the tag is effected without performing a cache fetch.

Support for this amendment may be found throughout the specification, but specific reference is made to paragraph [0061] of applicant's published application (approximately page 15 as filed), wherein it is noted that applicants' invention is an improvement over prior art systems because:

"prior art switching suffers either excessive memory consumption requirements if a switch monitor as described in May, op. cit., is used wherein a switch entry is associated with each instruction address, or from massive hardware requirements if all known entries are to be stored in a CAM memory structure, or from slow performance if all migrant instruction addresses must be read from cache/memory. The present invention improves on these prior techniques because the determination of whether a translation exists can be effected by the relatively fast technique of examining a field within the code tag associated with an instruction, rather than perform a cache fetch for possible translated versions in each case. Therefore, the current invention improves switch detection and translation without unduly degrading performance or posing massive hardware requirements."

This is in sharp contrast to Bala, wherein the tag "hits" are the presence of translated code in a cache (see Bala, column 1, lines 43-48 and column 3, lines 22-30).

In view of the above, it is respectfully submitted that claim 1 is directed to patentable subject matter.

Apparatus claim 11 has been amended in a manner analogous to method claim 1. For the reasons set forth with respect to claim 1, it is respectfully submitted that claim 11 is also directed to patentable subject matter.

The remaining claims depend from one of the independent claims discussed above. These claims have further recitations, which in combination with those of the claim from which they depend, are not taught or suggested by the art of record.

It is respectfully submitted that the Examiner is simply wrong with respect to claims 7 and 17, which recite that the tag is represented by a single bit. Reference is made to Bala, column 3, and throughout. The undersigned could find no teaching or suggestion that the cache hit signal is a single bit signal. In fact the teachings of column 3 of Bala seem to suggest that cache hit or miss signals would have more than a single bit. The Examiner admits as much in the rejection of claims 8 and 18.

Respectfully submitted,

David Aker
David Aker, Reg. No. 29,277
23 Southern Road
Hartsdale, NY 10530

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Date

Tel. & Fax 914 674-1094